ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

CURRENT STARVED VCO DESIGNED USING 70NM CMOS PROCESS

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DOI: 10.5281/zenodo.47045

ABSTRACT

Current starved VCO is simple ring oscillator consisting of cascaded current starved inverters. This paper gives a performance evaluation of five staged Current Starved VCO on simulating tool Tanner 13.0 using 70nm CMOS Process Technology. Performance evaluation is done in terms oscillation frequency, average power consumption, and tuning range. The Frequency has been enhanced up to 2.6011GHz at $1.8V_{DD}$ with low power consumption of 170uW. The tuning range in five stage current starved VCO is come out to be high ranging from 0.1 to 1.8V. This design is highly suitable for PLL applications. Therefore, a robust VCO can be designed for reliable operation. The techniques proposed in this paper can also be applied to other low voltage analog and RF circuits to improve their performance.

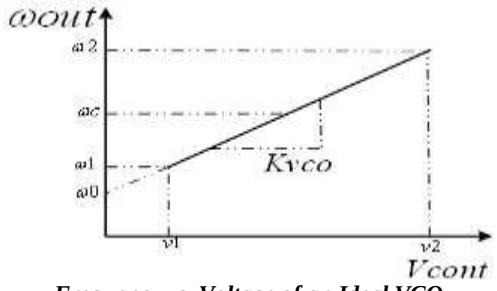
KEYWORDS: Current starved VCO, Tanner, five staged, High Frequency, Low Power and High Tuning Range.

INTRODUCTION

Oscillators are circuits that produce specific, periodic waveforms such as square, triangular, saw-tooth, and sinusoidal. They generally use some form of active device, lamp, or crystal, surrounded by passive devices such as resistors, capacitors, and inductors, to generate the output. There are two main classes of oscillator: relaxation and sinusoidal. Relaxation oscillators generate the triangular, saw-tooth and other non-sinusoidal waveform [1]. Sinusoidal oscillators consist of amplifiers with external components used to generate oscillation, or crystals that internally generate the oscillation. Sinusoidal oscillators consist of amplifiers with RC or LC circuits that have adjustable oscillation frequencies, or crystals that have a fixed oscillation frequency. Relaxation oscillators generate triangular, saw-tooth, square, pulse, or exponential waveforms. [2]

A Voltage Controlled Oscillator (VCO) is a device that produces alternating current whose frequency varies as a function of a DC voltage or current. The output frequency is altered by changing the control voltage or current. An ideal VCO has a linear change in the output frequency as the voltage changes linearly. The VCO is a useful circuit because its oscillation frequency can be set to a desired value. The gain (K_{vco}) or sensitivity of a VCO is defined in equation (A). The gain is the slope of the frequency change over the voltage change. [25]

$$K_{vco} = (F_{max} - F_{min}) / (V_{max} - V_{min}) \quad \text{(A)}$$



Frequency vs. Voltage of an Ideal VCO

The output frequency of a VCO is noted as ω_{out}, which is defined in equation (B), [6]

$$\omega_{out}=\omega_o+K_{vco}*V_{cont} \quad \text{.....(B)}$$

V_{cont} is the control voltage, and ω_o is the frequency when the control voltage is zero (if an oscillation is still possible at zero).visually defines, $K_{vco,}$ ω_{out} and ω_0 . K_{vco} is the gain of the VCO that controls how much a change in control voltage will change the VCO's frequency. $V_{control}$ is the input to the VCO that sets it to the desired frequency. It is this tunability that makes the VCO such an important and useful circuit. [17]

A CMOS Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. VCO constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency selection and signal generation. Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. Their output frequency is a function of a control input usually a voltage. Most application required that oscillator be tunable, i.e. their output frequency be a function of a control input, usually a voltage.[13]

They are commonly investigated circuit due to its use in phase-locked loops (PLLs) and clock and data recovery circuits (CDRs). As mixed-signal systems increase in popularity, more complex analogue circuitry must be designed in standard digital CMOS processes. VCOS fabricated in CMOS have typically been composed of current-starved ring oscillators, which have limited control over the operating and centre frequencies. The VCO presented in this Letter overcomes these limitations through the implementation of a current-steering trans-conductance amplifier and a current-to-frequency oscillator.

A. Advantage Of Using Current Starved VCO

There are two different types of voltage controlled oscillators used in PLL, Current starved VCO (ring oscillator) and Differential VCO. In recent years LC tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an *LC*-oscillator (around 10 - 20%) is relatively low when compared to ring oscillators (>50%). So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. [19] For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three. Therefore, some extra processing steps may be required. Finally, on-chip spiral inductors occupy a lot of chip area, typically around 200 ×200-300 ×300 m2, which is undesirable for cost and yield consideration. The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. Thus the chip area is reduced. In addition to a wide tuning range; ring oscillators with even number of delay cells can produce quadrature-phase outputs. The phase noise performance of ring oscillators is much poorer in general. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which a key requirement for battery operated devices.

The different performance parameters that distinguish one VCO from another are the following: center frequency, tuning range, lock range, tuning linearity, output amplitude, power dissipation, and signal output noise.

B. Types of VCO

There are typically three types of voltage controlled oscillators; (1) the traditional (inductor/capacitance) LC oscillator, (2) the non-LC oscillator, and (3) oscillators containing special components making variable oscillation possible. They can be oscillators containing electromechanically tunable capacitors, and MOS varactor transistors. [22]

I. LC Oscillators

The traditional LC VCOs are the most popular for a number of reasons. They do not require a special, expensive fabrication process, unlike some of the electromechanically tunable capacitors or varactor transistors. The signal to noise ratio is typically higher than that of a phase lock loop. The Q values achieved by LC oscillators are superior to the other types of oscillators in the quality for the amount of design effort and cost of fabrication. They also do not require an external clock signal.

The oscillation is created from negative feedback which causes the circuit to be unstable. The instability eventually causes a phase shift. When the $V_{control}$ is changed on a traditional VCO the amount of negative feedback is

proportionally changed. The result is an output frequency that varies. The tuning range is typically smaller compared to the other types of oscillators.

II. Non-LC Oscillators

The non-LC oscillators have characteristics similar to a digital circuit. They behave like an analog circuit, but have similar characteristics to that of a digital design. There are two types of non-LC VCOs.

1. Current starved oscillator, and
2. Second is a technique called Interpolation

The advantage of the non-LC Oscillators is their wide tuning range. Their tuning range can be as large as three times the tuning range of the LC VCOs. They also are easy to design. These two properties make them popular. The disadvantage the non-LC oscillators have is the relatively high phase noise. This is due to the circuit not containing any passive resonant elements.

III. Special Components

Another method of creating a VCO is to use a traditional oscillator topology and electrically alter the properties of the components. This technique makes it possible to build a complex circuit with a simple topology. It also has the capability of producing extremely high Q values.[10,9] The special components often require special fabrication processes or post-fabrication alterations. They can be

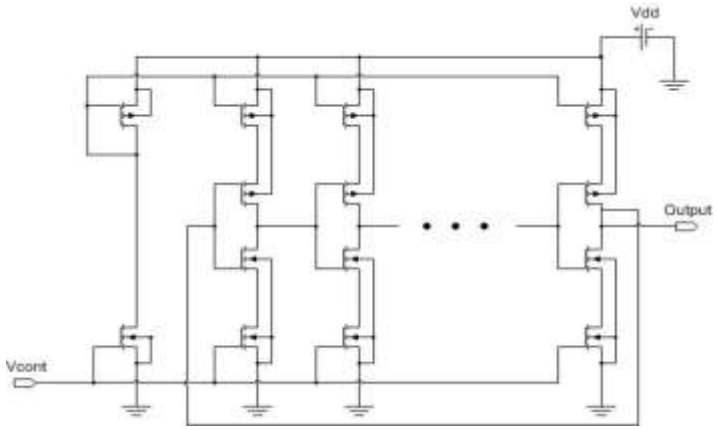
1. Tunable Diode
2. Varactor Transistor (Varactor capacitance)

C. Current Starved Oscillator

The current starved VCO works similar to ring oscillator. A VCO is implemented using a ring oscillator with a slight modification. The standard ring oscillator is modified by replacing inverters with current-starved inverters (also called ring inverters). The frequency of the VCO is determined by the delay of a ring inverter. The delay of each ring inverter is controlled by the varying gate voltage $V_{control}$ of its current starved transistor. The maximum discharge current (and hence delay of the ring inverter) is limited by the current starved transistor. Lowering $V_{control}$ reduces the discharge current and hence increases the propagation delay. The ability to alter the propagation delay per stage allows us to control the frequency of the ring oscillator structure. The most basic of these circuits is the current-starved CMOS inverter. This is based on a simple CMOS ring oscillator. In order to convert a ring oscillator into a VCO, the total propagation delay must be changed. There are two ways:-

1. Varying the Load
2. Varying the current drive of the inverters.

Adjusting the current causes the effective propagation delay of the inverters to be changed, which changes the frequency of the circuit.



A Full Current Starved VCO topology

The VCO in figure is a basic ring oscillator with three inverters forming the ring. The transistor that changes the amount of current that flows through the ring is the NMOS transistor that has Vcont as an input into the gate. When V_{cont} is at V_{dd}, the full current is able to flow to the ring oscillator. As the voltage is lowered, the current through the ring oscillator is limited. The buffer at the end of the circuit pulls the signal back up to V_{dd}.

CIRCUIT DESCRIPTION

Five Staged Current Starved VCO

A five staged Current-Starved VCO is shown in figure. Each delay cell consist of one PMOS and NMOS which operate as inverter, while upper PMOS and lower NMOS operate as current sources. The current sources limit the current available to the inverter i.e. the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter current source stage. PMOS and NMOS drain currents are the same and are set by the input control voltage. The total capacitance C_{total} is given by,

$$\mathbf{C_{total}} = \frac{5}{2}\mathbf{C_{ox}(W_pL_p+W_nL_n)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (1)$$

Where C_{ox} is the oxide capacitance. The number of stages of the oscillator is selected as 5 stages.

The centre drain current is calculated as:

$$I_{Dcentre}=N*V_{DD}*C_{total}*F_{centre} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$

where N is the number of stages of inverter.

The sizes of PMOS and NMOS of inverter stage are determined as:

$$I_{Dcentre}=\frac{\beta}{2}(V_{gs}-V_{thn})^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

Where, $\beta = K_p * \frac{W}{L}$

The oscillation frequency is: $F_{osc}=\frac{1}{N} * T_d$ …..………….. (4)

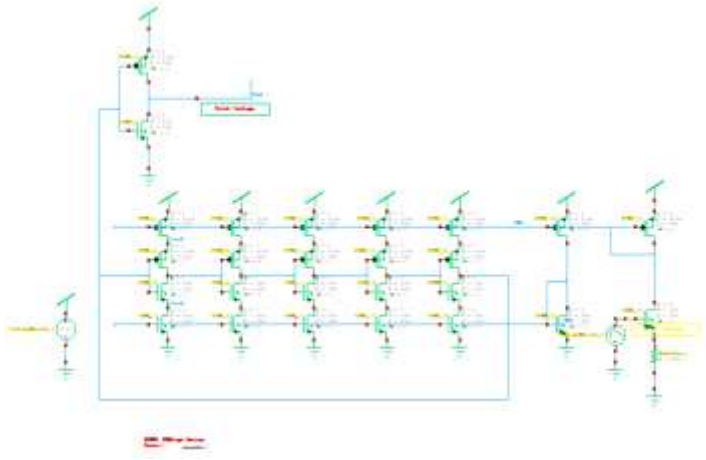
$$F_{osc}=I_D*C_{total}*V_{DD} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

where T_d is the time delay.

Above equation gives the centre frequency of the VCO when $I_D=I_{Dcentre}$. The VCO stops oscillating, neglecting sub-threshold currents, When, $V_{inVCO}<V_{thn}$. Thus, $V_{min}=V_{thn}$ and $F_{min}=0$ .The max VCO oscillation frequency F_{max} is determined by finding I_D when $V_{inVCO}=V_{DD}$[5].

The circuit simulation on TANNER Tool using S-edit is as follows:

ISSN: 2277-9655
(I2OR), Publication Impact Factor: 3.785



Circuit Diagram for 5 Staged CSVCO

PERFORMANCE COMPARISON

According to the design topologies in this paper, the performances of five staged VCO is evaluated on the parameters such as i/p tuning range, range of oscillation frequency, and power consumption with a qualitative discussion by an analytical approach. Table I shows the performance parameter computation of current starved VCO. Considering the minimum channel length and width of the device. Thus it can be seen that through VCO we can achieve wide tuning range and frequency range with low power consumption for PLL.

Table 1: Measured Performances

Parameters	5 staged current starved VCO
Tool	Tanner 13.0V
Technology	70nm
Power Supply (V_{dd})	1.8 V
Input tuning Voltage range	0.1 – 1.8 V
Range of oscillation frequency	183.48MHz – 2.6011GHz
Power consumption	170uW
Centre Frequency	1.39233 GHz
No. of delay cells	05
Gate length	70nm

The relationship between control Voltage and Frequency can be summerized by ploting the graph showing voltage against frequency.

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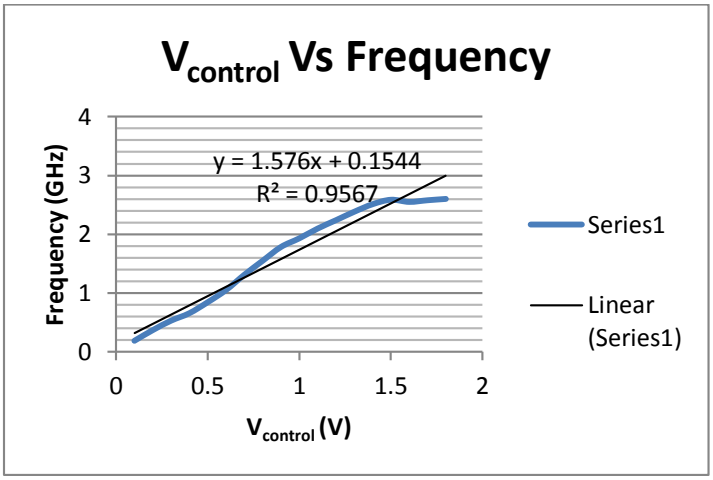

Graph 1: Control Voltage Vs Frequency

Table 2: $V_{control}$ Vs Frequency

S.No	Vcontrol (V)	Frequency (GHz)
1	0.1	0.18348
2	0.2	0.36496
3	0.3	0.52631
4	0.4	0.65359
5	0.5	0.84033
6	0.6	1.04766
7	0.7	1.3085
8	0.8	1.54707
9	0.9	1.7823
10	1	1.9296
11	1.1	2.09599
12	1.2	2.2387
13	1.3	2.38276
14	1.4	2.51136
15	1.5	2.5873
16	1.6	2.5503
17	1.7	2.57864
18	1.8	2.60118

CONCLUSION

This paper evaluates the performance of 5 staged current starved VCO for PLLs, with the design experiment and with the qualitative evaluation. Our measurement results show that maximum frequency comes out to be 2.6011 GHz and in case of power consumption and tunable frequency range, 5 staged Current starved VCO is better with other designs. Power consumption and chip area of PLLs will decrease proportional to the technology node. However, noise characteristics will get worse as inversely proportional to the technology node. The techniques proposed in this paper can also be applied to other low voltage analog and RF circuits to improve their performance. This designed VCO can be used as frequency synthesizer, frequency multiplier and for clock systems design.

REFERENCES

1. B .Razvi, Design of ANALOG CMOS Integrated Circuits, McGraw- Hill, 2001.
2. Harvinder Singh Saluja, Abhishek Choubey, Abhishek Jain, "A Single Stage Source Coupled VCO in 0.18µm CMOS Technologies with Low Power Consumption", International Journal of Computer Technology and Electronics Engineering (IJCTEE).
3. William Shing, Tak Yan, and Howard Cam Luong, ―A 900-MHz CMOS low-phase- noise voltage-controlled ring oscillator, IEEE Transactions on Circuits and System II: Analog and Digital Signal Processing,, vol. 48, pp. 216-221, Feb. 2001.
4. T. H. Lee and A. Hajimiri and, ―Oscillator Phase noise: A tutorial, IEEE J. Solid-State Circuits, vol. 35, pp. 326–336, March 2000.
5. T. C. Weigandt, B. Kim, and P. R. Gray, ―Analysis of timing jitters in cmos ring oscillators, In Proc. ISCAS, pp. 27-30, June 1994.
6. R. Jacob Baker, Harry W. Li & David E. Boyce, CMOS Circuit Design Layout, and Simulation, IEEE Press, 2002.
7. Haripriya Janardhan,Mahmoud Fawzy Wagdy, "Design of a 1GHz Digital PLL Using 0.18µm CMOS Technology" in IEEE 2006 Third International Conference on Information Technology: New Generations (ITNG'06).
8. D. A. Badillo and S. Kiaei, ―A low phase-noise 2.0 V 900MHz CMOS voltage controlled ring oscillator, Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 international Symposium on Volume 4, 23-26 May 2004 Page(s): IV - 533-6.
9. D. P. Bautista and M.L. Aranda, ―A low power and high speed CMOS Voltage-Controlled Ring Oscillator, Circuits and Systems, 2004. ISCAS '04.Proceedings of the 2004 International Symposium on Volume 4, 23-26 May 2004 Page(s): IV - 752-5 Vol.4.
10. H. Z. Lei, High Frequency Phase-Locked Loop Design and Simulation, Thesis (B.S.), California Polytechnic State University, 2004. Microfiche. San Luis Obispo, Calif. : MPI Microfilm Service,2004
11. Y. Limdulpaiboon, "A Phase-Locked Loop Circuit Design and Implementation", Thesis (B.S.),California Polytechnic State University, Microfiche. San Luis Obispo, Calif. MPI Microfilm Service, 2003.
12. S. Brown and Z. Vranesic, Fundamentals of Digital Logic with VHDL Design, ISBN 0071161686, Dept. of Elec. & Comp. Engineering, University of Toronto, 2000
13. M. Suresh, Design of a Testable Jitter-Free Digital Phase-Locked Loop, Thesis (M.S.), Santa Clara University, School of Engineering, 1996.
14. D. H. Wolaver, Phase-Locked Loop Circuit Design, N.J, ISBN 0136627439, c1991. *for All Digital Phase-Locked Loops* Hindawi Publishing Corporation VLSI Design Volume 2010, Article ID 946710"
15. Herzel, F.; Pierschel, M.; Weger, P.; Tiebout, M. "Phase Noise in a Differential CMOS Voltage-Controlled Oscillator for RF Applications." IEEE Transactions on Circuits and Systems - II, Volume: 47 Issue 1 January 2000.
16. Kato, K.; Sase, T.; Hideo, S.; Ikushima, I.; Kojima S. "A Low-Power 128-MHz VCO for Monolithic PLL IC's." IEEE Journal of Solid-State Circuits, Volume 23, Number 2 April 1988: 474-479. .
17. Lee, Thomas. The Design of CMOS Radio-Frequency Integrated Circuits. New York: Cambridge University Press, 1998. [19]. Gray, Paul, P. J. Hurst, S. H. Lewis, and R.G. Meyer. Analysis and Design of Analog Integrated Circuits. John Willy & Sons, Inc. 2001.
18. Baker, R. J., H. W. Li, and D. E. Boyce. CMOS Circuit Design, Layout, and Simulation. IEEE Press. 1998.